Md Kamrul Islam

Dhaka, Bangladesh • +880 1836 232 647 • md.kamrul.islam20feb@gmail.com
LinkedIn: www.linkedin.com/in/mdkamrulislam20

Professional Summary

Design Verification Engineer with 3.5+ years of hands-on experience verifying complex IPs across RTL and gate-level domains. Delivered end-to-end verification for DDR, USB PD Controller, RTC IPs, identifying 30+ silicon-critical bugs and achieving >95% coverage closure ahead of milestone deadlines. Proficient in Synopsys VCS, Synopsys Verdi, Cadence Xcelium, Cadence vManager and ModelSim, with strong scripting skills in Bash and Python to automate regressions and cut debug cycles by 30–40%.

Professional Experience

Ulkasemi Pvt. Limited — Dhaka, Bangladesh

Trainee Engineer (Feb 2022–May 2022) → *Assistant Design Verification Engineer (Jun 2022–Dec 2023)* → *Design Verification Engineer (Jan 2024–Dec 2024)* → **Senior Design Verification Engineer (Jan 2025–Present)**

DDR5 MRPHY GLS based Verification (Synopsys Inc. – Ulkasemi Client) (Nov 2024 – Present)

- Executed multi-corner GLS regressions for DDR PHY IPs at both RTL and gate-level, identifying and resolving 20+ timing, X-propagation, and functional issues critical for tape-out milestones.
- Modified enhanced UVM test benches and verification environments to match evolving chip requirements, ensuring functional coverage closure.
- Generated optimized VCD waveforms for power analysis and developed automation scripts, cutting GLS debug cycles by 30–40% and accelerating closure.

GLS Readiness & Testbench Refactoring (EXO Imaging – Ulkasemi Client) (Aug 2024 – Nov 2024)

- Re-engineered a client's UVM test bench for gate-level verification compliance; uncovered 12 latent netlist bugs and improved quality of results.
- Implemented Bash-driven regression automation to support continuous integration, reducing manual setup by 50% and enabling nightly GLS runs.
- Partnered with design team to identify root causes of 12+ complex GLS failures, cut debug turnaround time by 30%.

Real-Time Clock (RTC) IP Verification (Ulkasemi Internal Project) (Nov 2023 – May 2024)

- Authored comprehensive test plans, coverage models, and assertion libraries for a complex RTC IP, aligning verification tasks with chip requirements and achieving 90% functional coverage and 100% code coverage with documented waivers.
- Built a reusable UVMF environment leveraging UVM and UVM RAL to streamline register access and accelerate test development, catching 25+ functional bugs, reducing time to verification by 30%.
- Mentored 6 junior engineers on UVM and coverage analysis, accelerating their onboarding by 6 weeks and improving overall team verification throughput.

USB Power Delivery (PD) Controller Verification (Texas Instruments – Ulkasemi Client) (Sep 2022 – Jul 2023)

- Conducted verification of USB PD Controller sub-systems, constructing a robust UVM test environment and writing 100+ constrained-random test cases to exercise state machines and timing paths across RTL and gate-level simulations.
- Developed global checkers and scoreboards that caught 25+ functional bugs pre-silicon, directly contributing to first-silicon success.
- Executed GLS using Cadence Xcelium across multiple SDF corners, ran regressions using Cadence vManager to identify failure signatures and collaborated closely with design teams to ensure verification sign-off.

Wishbone-I2C & AMBA APB, AHB Verification Projects (Training) (Mar 2022 – Aug 2022)

- Architected multi-agent UVM test bench for Wishbone-I2C and single-agent UVM test benches for AMBA APB, AHB interfaces, developed detailed test and coverage plans, and achieved >90% functional coverage.
- Automated regressions with Python scripts, delivering a 30% reduction in test cycle time and establishing repeatable verification workflows.

Skills

- **Verification Concepts:** Functional Verification, Gate Level Simulation (GLS), Assertion-Based Verification
- **Methodologies & Languages:** UVM, SystemVerilog, UVM RAL
- **Protocols & IPs:** DDR PHY, USB PD Controller, RTC, DFI, AMBA (APB, AHB), I2C, SPI, PCIe Basics
- **Simulation & EDA Tools:** Synopsys VCS, Synopsys Verdi, Cadence Xcelium, Cadence Simvision, Cadence vManager, ModelSim
- **Scripting & Automation:** Bash, Python
- **Version Control & Project Tools:** Git, Perforce, JIRA

Education

- Master of Science in Electrical & Electronic Engineering – BRAC University, Dhaka, Bangladesh, Expected 2025
- Bachelor of Science in Electrical & Electronic Engineering – BRAC University, Dhaka, Bangladesh, 2020 (CGPA: 3.51)

Training & Certifications

- Gate-Level Simulation Training, VLSIGuru, 2025 – Focused on GLS fundamentals, testbench setup, SDF timing simulations, and power-aware verification basics.
- UVM-Based Verification Training, Ulkasemi Pvt. Limited, 2022 – Concentrated on IP testbench architecture, coverage-driven verification, and Python regression automation.