Md Kamrul Islam

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OBJECTIVE / GOALS

To pursue a PhD in Electrical and Computer Engineering with a focus on ASIC design and verification, where I can leverage almost 4 years of industrial UVM/GLS experience to develop scalable verification methodologies for high-speed and security-critical SoCs, and contribute to research at the intersection of hardware reliability, security, and AI/ML for EDA.

RESEARCH INTERESTS

Variation-aware Low-power VLSI | AI/Neuromorphic Accelerators | Secure and Reliable SoC Architectures | ASIC Design and Verification

EDUCATION

B.Sc. in Electrical and Electronic Engineering — 01/2016 – 12/2020
BRAC University — Dhaka, Bangladesh
CGPA: 3.51/4.00
Concentration: Electronics and Power, **Minor:** Computer Science
Thesis: **Outdoor Performance Analysis and Prediction of Photovoltaic Modules**
Advisor: **Md. Mosaddequr Rahman, PhD,** Professor and Chairperson, Department of EEE

PUBLICATIONS

1. M. M. Hasan Shawon, S. Akter, **M. K. Islam**, S. Ahmed and M. M. Rahman, "**Forecasting PV Panel Output Using Prophet Time Series Machine Learning Model**," 2020 IEEE Region 10 Conference (TENCON), Osaka, Japan, 2020, pp. 1141-1144, doi: 10.1109/TENCON50793.2020.9293751.
2. S. Akter, M. M. H. Shawon, **M. K. Islam**, S. Ahmed and M. M. Rahman, "**Degradation of PV Module Performance Due to Dust Accumulation on the High-rise Buildings**," 2020 IEEE International Women in Engineering (WIE) Conference on Electrical and Computer Engineering (WIECON-ECE), Bhubaneswar, India, 2020, pp. 239-242, doi: 10.1109/WIECON-ECE52138.2020.9398017.
3. S. Ahmed, **M. K. Islam**, M. Islam and M. M. Rahman, "**Short Term Performance Investigation of Solar PV Module: A Machine Learning Based Approach**," 2020 IEEE 8th R10 Humanitarian Technology Conference (R10-HTC), Kuching, Malaysia, 2020, pp. 1-6, doi: 10.1109/R10-HTC49770.2020.9357027

AWARDS, RECOGNITIONS & PARTICIPATIONS

1. Recognition by Ulkasemi Pvt. Limited that goes "**Exceptional Effort Beyond Regular Duties**" for tireless effort and commitment to outstanding contribution for the team and the organization in **2025.**
2. Given a **Letter of Appreciation** for **dynamic and insightful participation** in the **5th Alumni Advisory Panel (AAP) Meeting** held by the Department of Electrical and Electronic Engineering, BRAC University on October 11 **2025.**
3. Promoted to **Senior Engineer** by ULKASEMI Pvt. Limited for **leadership, knowledge and dedication** to the team and the organization in **2025**.
4. Promoted to **Engineer** by ULKASEMI Pvt. Limited for **outstanding performance, dedication and commitment** to the team and the organization in **2024**.
5. Achieved **1st Position** in an **Online Article Writing Contest** on **Electrical Engineering Research to Combat Corona Virus Pandemic** Powered by IEEE Power & Energy Society Bangladesh Chapter in **2020**.
6. Led a project - **Mohashunno project** in **Space Apps COVID-19 Challenge** organized by **Space Apps** in 2019.
7. Given a recognition of **excellent contribution** as an **Instructor** of workshop on **Basic Arduino** hosted by BRAC University Electrical & Electronic Club in **2018**.
8. **Finalist** of a technology-based Business Competition **TechBeez** arranged by LightCastle Partners in **2017**.

RESEARCH & PROJECT EXPERIENCES

1. **GLS-based Verification of DDR PHY IPs** **Synopsys, Inc. - Ulkasemi's Client | 11/2024 – Present**
   Target: Ensure gate-level sign-off readiness of DDR PHY IP through multi-corner GLS (SDF and 0-delay) and Gate-Level regression closure for tape-out milestones
   Responsibilities:
   - **Leading** a team of 1 engineer and 2 assistant engineers to **achieve set milestones** to meet the project deadline
   - Running multi-corner (**SDF MAX/MIN and 0-Delay**) **GLS regressions**
   - Debugging **timing**, **X-propagation**, and **functional** failures
   - Updating/enhancing **UVM testbench** and **verification environment** to match evolving IP
   - Generating optimized **VCD** deliverables for Design Implementation team for **Power analysis**
   - Writing **automation** scripts to streamline runs/debug
   - Maintaining the changes made in the codebase using **version control** tool **Perforce**
   - Reporting identified bugs and their fixes on **JIRA** for tracking the verification flow

   Outcome:
   - Identified/resolved **30+** tape-out critical **functional issues** across multiple products of **DDR PHY and reduced** GLS debug cycles by ~**30%** through automation scripts
   - **Distributed** tasks among the 3 assistant engineers and conducted **weekly meeting with client** to speed up the whole process and to meet the deadline

   Tools usage: SystemVerilog, UVM, **Synopsys VCS**, **Synopsys Verdi**, Perl, Python, Bash, Makefile, Perforce, JIRA

2. **Testbench GLS Readiness & Refactoring** **EXO Imaging - Ulkasemi's Client | 08/2024 – 11/2024**
   Target: Make RTL-provided linear testbench GLS-ready and establish a reliable, automated GLS regression flow
   Responsibilities:
   - Reviewed and **refactored linear testbench** for GLS compatibility
   - **Automated GLS** execution and run orchestration
   - Debugged multiple **X-propagation** and **compilation** issues to improve and stabilize pass rate

   Outcome:
   - Improved GLS readiness and regression stability
   - Reduced manual run effort and enabled repeatable GLS execution

   Tools usage: SystemVerilog, Cadence IUS, Cadence SimVision, Bash

3. **Real-Time Clock (RTC) IP Verification** **Ulkasemi Internal | 11/2023 – 05/2024**
   Target: Own end-to-end verification sign-off of RTC IP with strong functional/code coverage and reusable methodology
   Responsibilities:
   - **Developed verification plan** for **functional test, assertions and coverage** implementation
   - **Implemented testcases**, **UVM RAL** model, **coverage** model, and SystemVerilog **assertions**
   - Developed reusable **UVMF-style environment** to speed up register access and test development
   - **Reported functional bugs** and their fixes on **GitHub** to track the verification flow.
   - Maintained the changes made in the codebase using **version control** tool **Git**
   - Tracked waivers and drove closure with proper documentation

   Outcome:
   - Achieved ~**98% functional and code coverage** (with tracked waivers)
   - Caught **25+** functional bugs and confirmed fixes with RTL designer
   - Reduced verification time by ~**30%** by automating test runs using Bash

   Tools usage: SystemVerilog, UVM, Cadence Xcelium, SimVision, ICCR, IMC, Bash, Git, GitHub

4. **USB Power Delivery Controller IP Verification** **Texas Instruments - Ulkasemi's Client | 09/2022 – 07/2023**
   Target: Verify USB-PD controller sub-systems across RTL + Gate-Level Simulations and support first-silicon success through developing Constrained Random Tests, Global checker (assertions), Functional coverage model.
   Responsibilities:
   - Developed **testplan** for functional behavior of different block across the **sub-system**
   - Developed **80+ constrained random testcases** for state machines, and timing paths
   - Implemented global checkers using **SystemVerilog Assertions**
   - Ran and managed **regressions though Cadence vManager**
   - Executed multi-**corner (SDF Max, Min and Zero Dealy) Gate-Level Simulation** regressions

- Triaged **Gate-Level functional issues**, documented and reported their fixes
- Maintained the changes made in the codebase using **version control** tool **DesignSync**

Outcome:

- Found **25+** pre-silicon functional bugs
- Contributed to **first-silicon success**
- Improved regression triage/sign-off efficiency through structured failure signature analysis.

Tools usage: SystemVerilog, UVM, Cadence Xcelium, Cadence SimVision, vManager, Bash, Perl, DesignSync

5. **Outdoor Performance Analysis and Prediction of Photovoltaic Modules Using Machine Learning Algorithm** **Undergrad Thesis | 08/2019 – 06/2020**

Target: PV module performance under real weather conditions, quantify dust impact (clean vs. dusty), and predict PV current/energy using ANN/MLP models.

Responsibilities:

- **Designed** a rooftop **setup** with **two mono-Si PV** modules (clean vs. dusty)
- **Built** a Raspberry Pi–based **weather station** to **log** PV module output (Short-circuit current) and environmental data (temp, humidity, wind, pressure)
- **Derived solar irradiance** and prepared datasets (CSV) for modeling.
- Wrote **Python scripts** to collect, clean, and prepare data for training machine learning models.
- Developed an **ANN model** to predict the output of the mono-Si PV modules based on the trained dataset.

Outcome:

- Found **temperature** as the most correlated parameter with PV module output
- Achieved MLP prediction performance Short-circuit Current: clean panel avg. % diff -1.92% to 2.21% (RMSE 23.96–37.96) and dusty panel avg. % diff -7.32% to 13.35% (RMSE 22.11–61.22); **Energy:** clean **-1.87% to 7.9%**, dusty **-4.21% to 8.67%**
- Showed temperature-only inputs produced ~**0.76%** average difference in cumulative light energy vs. using all weather parameters (in the studied comparison).

Tools usage: Raspberry Pi 3B+, Arduino UNO, INA219, DS18B20, DHT11, BMP180, anemometer, PuTTY, TightVNC, Python, ANN

PROFESSIONAL EXPERIENCES

1. **Senior Engineer, Design Verification, Digital** **ULKASEMI Pvt. Limited | 01/2025 – Present**

Responsibilities:

- Lead and mentor a team of engineers/assistant engineers on **client projects**, including **recruitment**, **training**, task allocation, technical guidance, work reviews, and weekly client status/issue meetings.
- Own and drive the **verification plan**, **DV strategy**, and **sign-off** for **blocks/subsystems**, collaborating with **design/architecture** and **cross-functional teams** to clarify **specifications** and close issues.
- Architect and maintain **UVM testbenches**, implementing **functional coverage** and **assertions** and achieving **coverage closure** with justified waivers.
- Run and manage **regressions** and **GLS** activities, debugging complex **protocol/timing/corner** issues, supporting **integration**, **low-power/reset/clocking** scenarios, and driving **root-cause fixes** with design towards sign-off.

2. **Engineer, Design Verification, Digital** **ULKASEMI Pvt. Limited | 01/2024 – 12/2024**

Responsibilities:

- Executed **DV tasks** independently on **client projects**, supporting the **team lead** and participating in weekly **client meetings** to report status and discuss issues.
- Built and maintained **UVM tests**, **sequences**, and extended **agents/environments**; developed **directed** and **constrained-random tests** for **corner/error scenarios**; maintained **scoreboards**, **checkers**, **monitors**, and **reference models**.
- Drove **coverage closure**, ran **regressions**, debugged failures with **design/architecture** teams, and improved **automation** and overall **testbench stability**.

3. **Assistant Engineer, Design Verification, Digital** **ULKASEMI Pvt. Limited | 05/2022 – 12/2023**

Responsibilities:

- Assisted **team lead/senior engineers** in **verification tasks** by implementing **testcases/sequences** and small **UVM testbench** components, adding **assertions** and **coverage** items per DV guidelines and code style.
- Executed **regressions**, analyzed **failures** via waveforms/debug, reproduced and narrowed down issues, updated **test plans/logs/bug reports**, and collaborated with other teams when needed.

4. **Trainee Engineer, Design Verification, Digital** **ULKASEMI Pvt. Limited | 02/2022 – 05/2022**
Responsibilities:
   - Completed structured **training** on **SystemVerilog (SV)/UVM**, **simulation flow** (compile/run/debug), and the project environment; wrote and executed **smoke/sanity tests**, basic **sequences**, and small **utilities**.
   - Followed **training plans** and completed daily verification milestones for assigned practice projects.

5. **Student Tutor (EEE301), Department of EEE** **BRAC University | 06/2021 – 09/2021**
Responsibilities:
   - Conducted short classes on specific topics based on students' needs.
   - Assisted course faculty with recording marks for Quizzes, Mid, Final, Assignments
   - Helped weaker students overcome difficulties with particular topics.

TECHNICAL SKILLS

- **EDA / Simulation & Debug:** Synopsys **VCS**, Synopsys **Verdi**; Cadence **Xcelium**, Cadence **SimVision**, Cadence **vManager,** Cadence **ICCR,** Cadence **IMC**, Intel **ModelSim**
- **Verification & Sign-off:** Functional Verification, **Gate-Level Simulation**, **SystemVerilog Assertions**, Constrained-Randomization, Metric-/Coverage-Driven Verification**,** Regression
- **Hardware Description Languages & Methodologies: SystemVerilog**, Verilog, **UVM**, **UVM Register Abstraction Layer (RAL) Modeling, TLM**
- **Protocols / IP Exposure:** DDR PHY, USB-PD Controller, RTC, DFI, AMBA (APB/AHB), I2C, SPI, PCIe (Basics)
- **Scripting & Automation: Python**, **Bash**, Perl
- **Version Control / Tracking: Git**, **Perforce**, DesignSync, JIRA, GitHub
- **Programming:** Python, C/C++
- **Documentation / Tools:** MS Office, Excel, Adobe Illustrator, Adobe Photoshop

RELEVANT COURSEWORK

VLSI Design, Computer Architecture, Analog Integrated Circuit Design, Digital Electronics, Microprocessors, Programming Language I & II, Data Structures, Algorithms, Numerical Methods

STANDARDIZED TEST SCORES

IELTS - Overall 7.0, **Listening** 7.5, **Reading** 6.5, **Writing** 7.0, **Speaking** 6.0

TRAINING & CERTIFICATIONS

- **Gate-Level Simulation Training** by VLSIGuru - Focused on GLS fundamentals, testbench setup, SDF timing simulations, and power-aware GLS basics. 12/2024 – 07/2025
- Completed training modules on **DDR, DDR PHY**, **DFI**, and **GLS** during GLS-based DDR PHY verification project for Synopsys Inc. 11/2024 – 12/2024
- **UVM DV Training on Wishbone-I2C, APB-SPI & AMBA APB/AHB IP Verification** - Built a multi-agent UVM testbench for **Wishbone-I2C, APB-SPI** and single-agent for **APB/AHB**; authored test/coverage plans; achieved >90% functional coverage, and developed **Bash/Python** script automation to cut test cycle time ~30%. 02/2022 – 08/2022
- Completed "**Excel Skills for Business: Essentials**" course offered by Macquarie University on Coursera. 03/2021
- Completed "**Programming for Everybody (Getting Started with Python)**" course offered by University of Michigan on Coursera. 06/2020
- Completed "**Python Data Structure**" course offered by University of Michigan on Coursera. 07/2020

COCURRICULAR ACTIVITIES

- Director of Logistics, BRAC University Electrical and Electronic Club (BUEEC). (2019) 01/2019 – 12/2019
- Student Volunteer, International Conference on Energy and Power Engineering (2019) 03/2019
- Patrol Leader at Mirpur Siddhanto High School Scout Group 01/2010 – 12/2010